In the Specification

On page 9, paragraph 2:

As shown in Fig. 3, wafer 18 may have an optional upper intermetal dielectric (IMD) layer, for example, comprised of PECVD silane (SiH_4) oxide film ~~22~~32. PECVD silane (SiH_4) oxide film ~~22~~32 has a thickness of preferably from about 100 to 2000Å, and more preferably from about 300 to 1200Å.

On pages 11 and 12, paragraphs 2 and 3:

Specifically, the inventors have determined that the deposition of thermal CVD TEOS oxide on: (1) wafers 18 having an upper PE SiH_4 oxide film ~~22~~32 is about 25Å/second; and (2) wafers having an upper PE TEOS oxide film is about 29 Å/second. Thus, the inventors posit that there exists a competition in thermal CVD oxide deposition between PE SiH_4 oxide film ~~22~~32 coated wafer 18 and PE TEOS oxide film 16 pre-coated CVD chamber inner walls 14 (See Figs. 2 and 3).

Generally, there exists a competition in thermal CVD oxide deposition between a wafer surface with an upper PE oxide film having a first thermal CVD deposition rate, and a pre-coated PE oxide thin film inner wall of a CVD chamber, for example, having a second thermal CVD deposition rate that is greater than the first thermal CVD deposition rate. In the case of CVD chamber inner walls 14 that have been pre-coated with a thin film 16 with a relatively high thermal CVD deposition rate, the

thermal CVD reactant gases will be attracted, as at 22 of Fig. 2, towards pre-coated inner walls 14 more than towards the surface of wafer 18 having upper film ~~22~~32.